Design of A Programmable Bandgap Reference Circuit

Khadijeh Karamzadeh, Akaram Asghari Govar, Jafar Sobhi, Hamid Moharrami

Abstract— This paper describes the design of a programmable voltage bandgap reference, simulated in 0.35µm CMOS technology. This work is used for trimming and calibration process. The circuit generates a variable reference voltage of 1.2380 until 1.3051. It can operate with supply voltages between 3.0v and 3.6V and between 0C and 85C. It has a PSRR 56dB under normal operating conditions. This circuit works in a current feedback mode, and it generates its own reference current, resulting in a stable operation. A startup circuit is required for successful operation of the system.

Index Terms—Proportional To Absolute Temperature (PTAT), Conversely proportional To Absolute Temperature (CTAT), BandgapReferenc (BGR), Temperature Coefficient (TC).

1 INTRODUCTION

A KEY ELEMENT of analog-to-digital (A/D) and digital-to-analog (D/A) converters is a precise voltage reference with good temperature stability. Accurate biasing voltages are critical for many circuit schemes; in ADC, a reference voltage is required to quantify an input, while in DAC, it is required to define the output full-scale range. As a well-established reference generator technique, bandgap reference is most popular for both Bipolar and CMOS technologies.

The principle of the bandgap circuits relies on two groups of diode-connected BJT transistors running at different emitter current densities. By canceling the negative temperature dependence of the PN junctions in one group of transistors with the positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit which includes the other group of transistors, a fixed DC voltage which doesn't change with temperature is generated.[3][4] There are many different implementation reported, while essentially a bandgap reference circuit consists of a supply independent biasing circuit, a diode connected BJT transistor generating a voltage with negative temperature coefficient, a PTAT circuit and some kind of feedback mechanism to improve the performance. This working principle of a bandgap voltage reference can be illustrated by Fig1 since V_{BE} decreases approximately linear with temperature while V_T increases linearly with temperature, a low-temperature-dependence V_{REF} can be obtained by scaling up V_T and summing it with V_{BE}.

The outline of this paper is as follows: in section II circuit description is presented. Section III presents circuit analysis units. In the section V, we demonstrated simulation result. The results were obtained by simulation produce in a 0.35 µm processions form the last section.

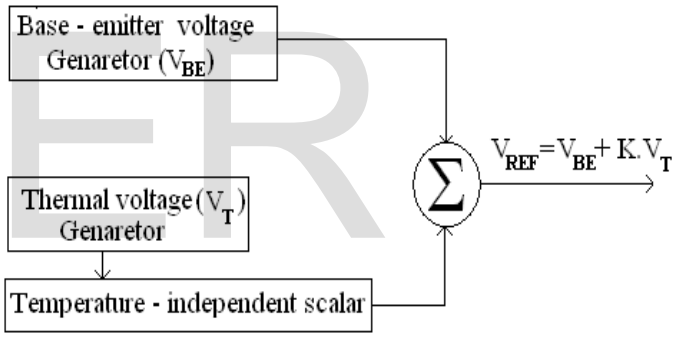

Fig. 1.Concept of bandgapVoltage Reference

2 CIRCUIT DESCRIPTION

Adding two voltages that have temperature coefficients of opposite sign with suitable multiplication constants generates a reference voltage. The resulting voltageobtained is independent of temperature. The diode voltagedrop across the base-emitter junction, VBE, of a BipolarJunction Transistor (BJT) changes Complementary toAbsolute Temperature (CTAT) [1]. Whereas if two BJTsoperate with unequal current densities, then the difference inthe base emitter voltages, ΔVBE, of the transistors is found tobe Proportional to Absolute Temperature (PTAT). The PTATrelationship is given by [2],

$$\Delta V_{BE} = V_T \ln m; \qquad V_T = kT/q \qquad (1)$$

where, k is Boltzmann's constant, T is the absolutetemperature, q is the electron charge and m is the ratio of thecurrent densities of the two BJTs. The PTAT voltage may beadded to the CTAT voltage with suitable

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weighting constantsto obtain a constant reference voltage.

It should be noted that in this section Rx is neglected. Fig.3 shows the block diagram of the variable badgap

times thecurrent density of the m BJTs identical to A, connected inparallel. The voltages at node X and Y are maintained at thesame value, VBE using a feedback network through adifferential amplifier. The voltages VBE and ΔVBE are addedtoobtain the reference voltage. The circuit also requires a startup circuit since there exists a stable state at which no current flows through the circuit. The startup circuit forces the transistors to turn on and the circuit to operate at its other stable state to generate the reference voltage.

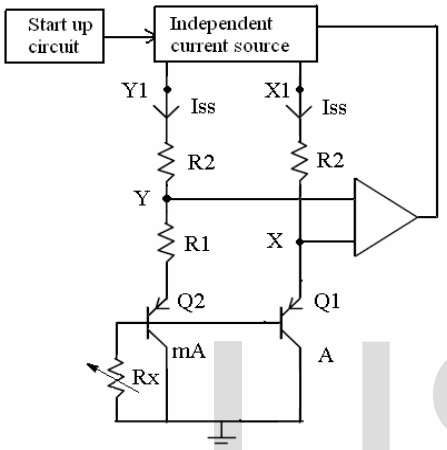


Fig. 2. Block diagram of Bandgap Reference Circuit.

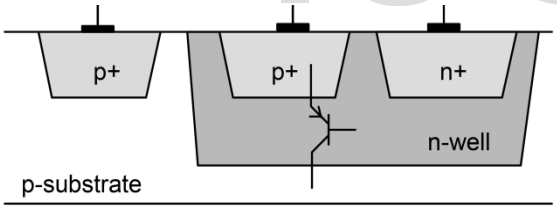
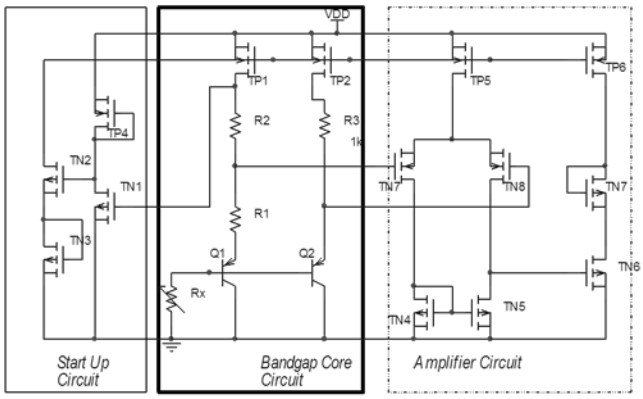


Fig. 3 .pnp BJT using CMOS process.



referencecircuit designed. By using a supply independent currentsource, a current ISS is passed through BJT A. The samecurrent ISS flows through m transistors connected in parallel,identical to A. Thus the current density of A is m

Fig 4: Schematic of Bandgap Reference Circuit showing the supply independent current source and generation of reference voltage.

It should be noted that an ideal BJT is not available in CMOS technology. A pnp BJT is made using the n-well normally associated with a PFET [1] the p-substrate behaving as the collector.

In order to generate supply independent current and carry out an addition of the CTAT and PTAT voltages, the circuit in Fig4 is used. The OPAMP provides the base voltage to the transistors, which are connected as current mirrors. By selecting the value of R1 and current ISS, the circuit may be designed to operate at the desired operating point. The value of R1 is given by,

$$R1 = \Delta V_{BE} / I_{SS} \quad (2)$$

Since the same current ISS flows through R2, the voltage at the output reference voltage nodes is given by,

$$V_{ref} = V_{BE} + I_{SS} R2$$

$$V_{ref} = V_{BE} + \Delta V_{BE} . \frac{R_2}{R_1} = V_{BE} + \frac{R_2}{R_1} . V_T . \ln m \quad (3)$$

Thus by selecting the value of R2 the weighting constant may be set. This arrangement provided an elegant arrangement to generate the reference voltage while conserving voltage headroom. The circuit has a stable operating point at which no current to flows through it. An arrangement must be made to force the saturation when the supply is turned on. The startup circuit carries out this function.

3 Circuit Analysis Units

3.1Bandgap Core

The bandgap reference voltage is generated by adding the base emitter voltage, VBE, of a BJT to the difference in base emitter voltage, ΔVBE of BJTs with a ratio of current density *m*. In order to generate a stable circuit, it is necessary to keep the BJT in the exponential region.

The change of the voltage of reference node is made possible by adding variable resistor in the base of Q1 and Q2 transistors. This method supplies the acceptable thermal characteristic to some extent (Fig4).

Ideally, the error amplifier has a high voltage gain A, and therefore $V_X = V_Y$ can be achieved, when R2=R3,

V_{DSTP1}=V_{DSTP2}can be easily obtained to provide a very good current matching by TP1 and TP2. V_{REF} can be generated by this structure without the need of an extra current branch. Both power consumption and errors can be reduced effectively.

The voltages X and Y are fixed by feedback, hence result the V_{REF} is given

$$V_{ref} = V_{BE} + I_{SS}.R_2 + \frac{I_{SS}}{\beta}.R_x \quad (4)$$

$$V_{ref} = V_{BE} + I_{SS}(R_2 + \frac{R_x}{\beta}) \quad (5)$$

$$V_{ref} = V_{BE} + \frac{\Delta V_{BE}}{R_1}(R_2 + \frac{R_x}{\beta}) \quad (6)$$

$$V_{ref} = V_{BE} + (\frac{R_2}{R_1} + \frac{R_x}{\beta R_1}).V_T.\ln m \quad (7)$$

In the order achieve a zero temperature coefficient; the following equation must be satisfied.

$$\frac{\partial V_{ref}}{\partial T} = (\frac{R2}{R1} + \frac{Rx}{\beta.R1})\ln m.\frac{\partial V_T}{\partial T} + \frac{\partial V_{BE}}{\partial T} \quad (8)$$

$$\frac{\partial V_{ref}}{\partial T} = 0 \quad (9)$$

$$\Rightarrow (\frac{R2}{R1} + \frac{Rx}{\beta.R1})\ln m.\frac{\partial V_T}{\partial T} = -\frac{\partial V_{BE}}{\partial T}$$

(10)

The equation shows that R1, R2, Rx and m affect on the TC of Vref. m is the ratio of the surface of Q1 and Q2 transistors. Because layouts on both BJTs and resistors should be well planned and designed so that consistent performance can be maintained with minimum need of trimming in mass productions. Better matching can be achieved by a common-centroid layout [6],[7]. However a large value of N is not preferred as the separation of devices increases, and this will introduce more errors. Moreover, as shown in (1) there is no signification increase on the ln(m) function when m increases.

For the resistor layout, common-centroid layout should be also used to obtain better matching[7]. Polysilicon is a better material than diffusion since its tempco is low. An even better material is high-resistive polysilicon, since it has a negative tempco. We used in the simulation.

As mentioned above, the amplitude of R1 and m are set before. Therefore only R2 and Rx are affected in the thermal characteristic. If R2 is much more than Rx/β, effect of the Rx in thermal characteristic would be neglected.

3.2Opamp

The OPAMP was used to maintain equal node voltages and provide a feedback to maintain the drain currents constant and insensitive to supply variations. A high gain of the OPAMP would result in better voltage tracking of nodes X and Y

(Fig4). The common mode voltages play an important role in determining the OPAMP topology. The input common mode was determined by the base emitter voltage of the BJT, which is 0.8 V at 100 μA of collector current. In order to meet the input common mode condition an active current mirror circuit with a PMOS driver was selected.

The output common mode voltage corresponds to the gate voltage of the current mirror transistors. In order to have a VDSAT of 0.4 V for these transistors the output common mode should be ideally about 1.5 V. A second stage was added to the OPAMP to increase gain and shift the common mode voltage up by using an NMOS driver. The NMOS driver only provided an output common mode of about 0.4 V. By adding a diode-connected transistor, TN7, to the second stage, the output voltage was pushed up to about 1.3 V without any effect on the gain of the stage. The voltage drop accress the diode connected transistor is about 1.2 V corresponding to VTH + VDSAT. The gain of each of the stages of the OPAMP is given by

$$A = gm.Ro \quad (11)$$

Where, Av is the gain, gm is the transconductance of the driving transistor and RO is the effective output resistance at the output node.

3.3 Startup Circuit

Transistors TN1, TN2, TN3 and TP4 constitute the startup circuit. Initially all the transistors start off in off state. The voltage at the gate of TN1 is low and so it remains in off state. TP4 being diode connected is always on and so the transistor TN2 turns on forcing the drain to a low value. The current mirror stack turns on and the gate voltage of TN1 rises and it starts to conduct. At this point there is a competition between the output of the amplifier TP6, and TN2 for the current source load. TN2 is designed to be a weak transistor so the amplifier takes control of the current mirror gate.

When the bandgap voltage is high enough (~1V) the transistor TN1 turns on. TN1 in linear region has to compete with TN2 in saturation so it is designed to be a big transistor. It draws all the current from TP2 and the base voltage of TN2 falls till it turns off. In this state the gate voltage at TN2 is about 0.6 V. This is high enough for the transistor TN1 to be conduct slightly. A diode connected transistor TN3 is added to increase the threshold voltage at the gate of TN3 to turn off. The transistor TP4 is designed to be a weak device

so that low current flows through the parasitic path when the circuit is in full operation.

4 RESULTS

The variable bandgap reference voltage gives a voltage of 1.2672V when adjusted to have a zero temperature coefficient at 27C when RX is 900Ω. Fig5 shows the result of the simulation. As can be seen an overall temperature coefficient of 0.0141mV/K is obtained between 0C and 85C, which corresponds to about 0.0946% variation. The response it worse for temperatures from 64-85˚C with a temperature coefficient of 0.0571mV/K. Below these temperatures the temperature coefficient is 0.01875mV/K.

Fig 6 shows the variation Vref when the Rx is varied from 1Ω to 2.4kΩ. The relative variation Vref is 2.79mv/kΩ at 27˚C. So the worst case operation of the device is when Rx is 2.4kΩ and 1Ω. In the table1, PSRR and TC are shown for different Rx.

Fig 7 shows variation of Vref when temperature changes between 0˚C to 80˚C. Temperature coefficient of 0.1mV/K is obtained.

The D.C characteristics at 80 degrees are shown in Fig 8. The variation with Vdd is much worse in this case. The simulation demonstrated PSRR is 37dB.

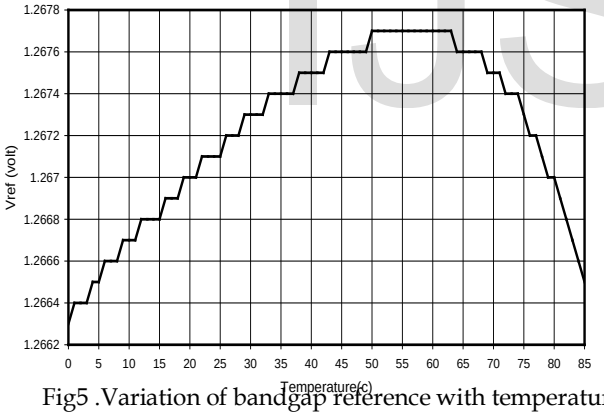


Fig5 .Variation of bandgap reference with temperature at Vdd=3.3V and Rx=900Ω

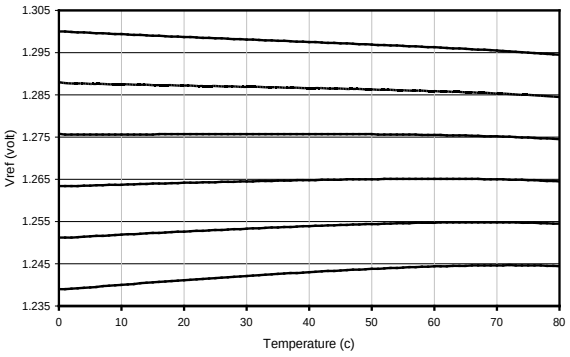


Fig6 .Variation of bandgap reference with temperature for Rx=1Ω to 2.4KΩ (Vdd=3.3V)

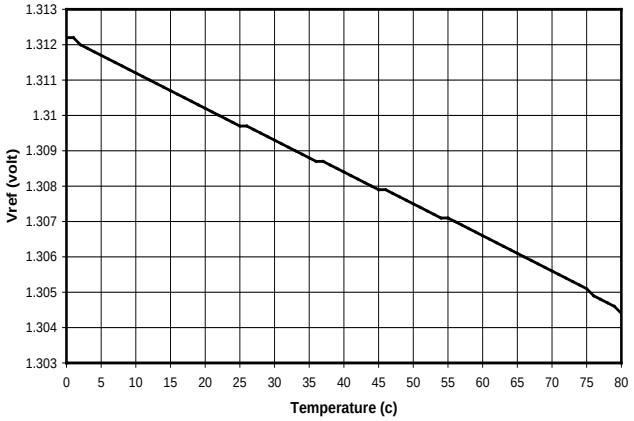


Fig7 .Variation of bandgap reference with temperature at Vdd=3.3V and Rx=2400Ω

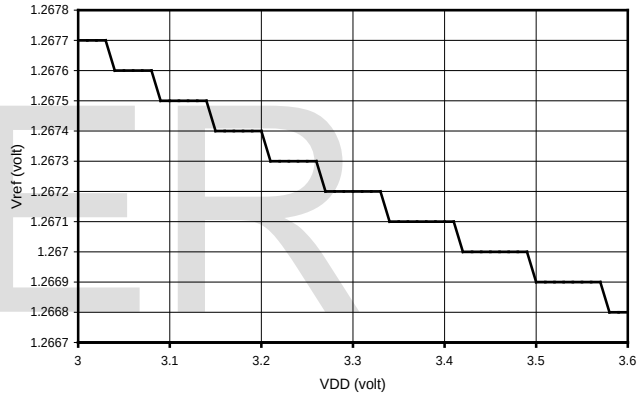


Fig8: Variation of the reference voltage with supply voltage at 27C

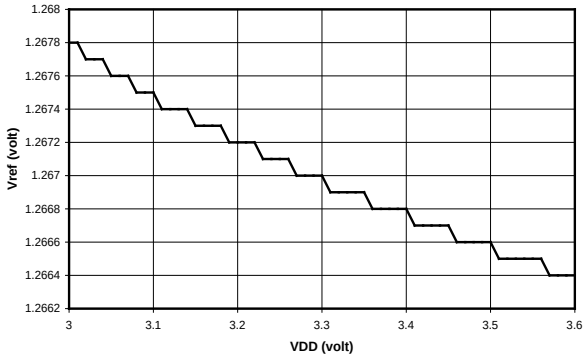


Fig 9: Variation with Supply Voltage at 80 C (absolute worst case)

TABLE 1

REFERENCE VOLTAGE OBTAINED UNDER DIFFERENT RX

	Rx=1Ω	Rx=0.9k Ω	Rx=2.4k Ω
PSRR(dB)	42	56	37
TC (ppm/°C)	13.1	10.84	15.01

TABLE 2

SUMMARY OF PERFORMANCE WITH AND WITHOUT Rx

	With Rx	Without Rx
Technology (µm)	0.35	0.35
Supply voltage range (Volt)	3.00-3.6	3.00-3.6
V_{REF} (Volt)	1.2672	1.2228
PSRR (dB)	56	60
Temperature coefficient (ppm/°C)	10.84	10.2
Integrated noise (µV/sqrt Hz)	0.156	0.154
Load Regulation (50kΩ-120k Ω)	*87.1µV/Ω*	*85.21µV/Ω*

This circuit is simulated for FF, SS, FS and SF model. PSRR for FF, FS, SF and SS corner was 52dB, 55dB, 56dB and 60db and TC also was 15, 10, 50, and 20 ppm/C. These results show that FS is worse case for this circuit.

5 Conclusion

A bandgap reference with a current feedback mode has been designed. The circuit uses no external current sources and is designed to have a zero temperature coefficient at 27˚C. The design is simulated implemented with 0.35µm CMOS process. The circuit generates a variable reference voltage of 1.2380 until 1.3051. Table 2 shows the summary of performance of proposed circuit. The output voltage is 1.2659V at the nominal operating condition of 27˚C temperature and 3.3V supply voltage. It has a temperature coefficient of 0.0141mV/K from 0-804˚C.

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